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AMAT - Applied Materials New Technology Announcement

EVENT DATE/TIME: JUNE 05, 2018 / 3:00PM GMT

OVERVIEW:

Co. announced a breakthrough in materials engineering that accelerates chip performance in the big data and AI era.

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PRESENTATION

Operator

Welcome to the Applied Materials conference call. (Operator Instructions) As a reminder, this conference is being recorded. I would now like to turn the conference over to Michael Sullivan, Vice President of Investor Relations. Please go ahead, sir.

Michael Sullivan - *Applied Materials, Inc. - VP of IR*

Good morning, and thank you for joining us. Today, Applied Materials is excited to be bringing you some important new technology to the semiconductor industry. Today's call is designed to give you more details, also to give you a chance to ask some related questions later. This call is not going to be financial in nature.

Joining me this morning is Kevin Moraes and he's the Vice President in Applied Semiconductor Products Group. Before we begin, please note that you can find a copy of today's presentation on the landing page of our IR website at appliedmaterials.com. We'd encourage you to read the Safe Harbor passage on Page 2 so that we don't have to. Also on the website, are animations that we've created to help you visualize how the new technology works. So what you'll see today is 2D. If you click on the website, you'll see the process flow, and you'll see how everything works in detail.

Before we begin, I'd like to make a calendar announcement. On Tuesday morning, July 10, Applied will be hosting an investor breakfast at the Yerba Buena Center in San Francisco. That will begin at 8:00 in the morning. After the breakfast, we would like to ask you to stay with us for the AI design forum. This is a major industry event that will feature world experts in artificial intelligence, systems architecture, chip design and semiconductor process technology. The event is going to be the first to outline the future of computing all the way from materials on the wafer to systems. The event is being held in conjunction with semi and SEMICON West, and it will run from about 9:00 a.m. to 2:00 p.m. After that, it will be immediately followed by the Bulls and Bears panel. You'll be getting some invitation information in the near future and feel free, of course, to reach out to Applied Materials team.

So with that, I would like to turn the call over to Kevin Moraes.

Kevin Moraes

Thank you, Mike. Hello, everybody. This is Kevin Moraes. I want to thank everybody for attending today's presentation. So I'm Kevin Moraes, I'm the Vice President of Product Management in our metal deposition and packaging business group. This is within our Semiconductor Products Group. Just as a way of introduction, I've been with Applied since about 2000 and I've been with the Metals Group since about 2004.

Today, we're really excited to be announcing a major change in our transistor contact and interconnect metal road map. We're actually introducing a complete suite of products for the fabrication of transistor contacts and interconnects, using for the first time, the metal Cobalt. And just to give you some perspective, this is the first time in over 20 years that a new metal wiring scheme to connect billions of transistors is being used or is being announced. The last change was the early adoption of copper in 1997. And this is another example of some innovative materials, which are in work that Applied Materials is doing to enable the fabrication of the high-performance chips to power the AI era.

So before we start, this is the -- there's some forward -- this presentation includes some forward-looking statements, and we have a brief disclosure here that you should be aware of. As Mike mentioned, this is also posted in the presentation. So with that introduction, I'm going to start the presentation just with one high-level slide to put this all in perspective and provide some context for our excitement about the semiconductor industry. So we are actually setting up the cusp of the biggest computing wave yet as we enter the AI era, driven by big data. This, of course, builds on the huge expansion of the market during the mobile era, driven by social medium and previously, the personal computer and Internet era. And actually we're in the early innings of the era of AI and big data and we expect the need for significant enhancement of performance for both processors as well as the capacity and latency of memory required to enable this new wave.

So moving to Page #4. Just as we are nearing this performance for these big data applications, AI applications, we start to see that classical Moore's Law has been slowing down. On this chart -- on the chart over here -- is a chart put together by John Hennessy and David Patterson. And you can see the performance, although there's been a huge improvement in performance over the years, the rate of performance gains has been slowing down as we reached the limits of Dennard scaling in critical areas. We have seen the limits of the Powellism being reach, and we're now just seeing a general slowdown on the performance gains every year. By the way, if you are curious or interested more about this, David Patterson is going to be a guest at the Applied Materials AI Forum on July 10 that Mike mentioned earlier.

So moving to Slide #5. Just another couple of slides on the overall framework. In the PC era, we actually saw a very few number of materials that were integrated and primarily using lithography scaling. There was a significant improvement in performance gains that were achieved. However, these performance gains have been slowing down and the cost efficiency of these performance gains have been reducing as customers have had to deploy schemes such as self-aligned double patterning and self-aligned quadruple patterning as well as EUV to continue litho scaling. In addition, the industry has made many architectural changes, for example, going from plain of the FinFET that have improved performance. However, the biggest change you'll see is in the materials. So in the early '90s and 2000s, there were very few set of materials that we used in some extra manufacturing. By the year 2000s, as we enter the mobile area, the number of materials have increased. In fact, Applied also introduced the Cobalt encapsulation product back then, as well as, of course, high-K metal gate had been blocked by that time as well.

But we see the biggest change really up in the future where you're going to see a significant increase in the number of materials used and likely the adoption of many exotic materials required to deliver the performance gains that are going to be required for this AI era.

So add one more slide to underline, and this is on Slide #6. One more slide to underline, what's different and what we are presenting today? As I previously described in the PC era 1, this was calculated by classic Moore's Laws shrink and easily integrate a few number materials to improve gains and the gains are typically described in terms of the chip performance, power, area and cost, commonly referred to as PPAC. These could also be done with single process systems. In era 2, where classic Moore's Law has been suddenly hit certain limits, we've had to get to more complicated processes and, in fact, this is associated with more integrated process systems, but however, the complexity was still fairly straightforward, so it could be done with changes on a few systems.

As we enter era 3, to enable further PPAC improvements, they're going to require the adoption of many more new and exotic materials. Furthermore, as these dimensions shrink, interface start to become a large part of the area of these materials, the volume of these materials and entering of these interfaces and these materials becomes a key requirement. It's in this era 3, where you're talking about new materials and, for example, the one we are describing today, which is Cobalt here for the transistor contact interconnect, you will see the need for the adoption of these Integrated Material Solutions. And what I mean by this is it's not just the integration of a single new process, but a suite of processes that are required to assist the integration and adoption of these new materials.

So that's what's different about this. This is the Integrated Material Solutions space for -- to enable these new materials in era 3.

Moving to Slide #7. At Applied, we actually have a suite of very successful platforms that have been used in the semiconductor manufacturing for many, many years. In fact, virtually every chip made today has been made in one of these platforms, and we can build on these platforms.

So moving to Slide #8. We see that these platforms themselves have evolved in how they've been used. On the left-hand side is an example of the Endura platform that was typically used in era 1 and 2, and these were fairly straightforward single-purpose systems, typically having 1 or, at the most, 2 kinds of chambers or technologies integrated on that high-vacuum platform. But in era 3, and as for -- in this example of Cobalt-filled solution we described today, just on the Endura platform, it takes 4 unique processes, 1 ALD, 2 PVD and 1 CVD process, all integrated under vacuum to reliably fill Cobalt into very small features.

Slide #9. So at Applied, actually, we have the largest set of material engineering capabilities available to use. And this is really important. These -- integrating these new materials is going to require different kinds of dry-cleans, different kinds of deposition technologies, PVD in some cases, CVD and ALD in other cases. It requires innovations in planarization and etching, wet-clean and in some cases, modification of these materials. Applied is uniquely positioned to solve these new integration of problems and to bring these integrated material solutions to market. Then this is going to be required where you get higher performance out of chips.

So with that background, I want to talk about the metal today that we are introducing of the new change today. And this is really the biggest change in the transistor contact interconnect, as I mentioned, in 20 years. So we're actually introducing Cobalt as a metal solution. And this replaces, in certain cases, copper metal and in other cases, tungsten metal that are used today in the logics space. Cobalt is introduced because it has a lower resistance at smaller dimensions. It has excellent ability to fill small features. It can actually work with much thinner barriers and so it can have a large volume in the available space. It actually also has improves reliability versus copper and this happens to be a very big challenge to extending copper interconnects at small dimensions. At a capital, Cobalt as a metal is fab-friendly. And what I mean by this is when the industry moved to copper about 20 years back as an interconnect metal, they had to go through a significant change in the protocol as copper -- protocol required handle copper. Copper is quite detrimental to the transistor and copper defuses quite easily into dielectrics as well. And so that was a major change. But unlike copper, which was fast moving, Cobalt is quite benign and has, for some time in the past, been used in the front-end or close to the transistor level. So it's a relatively easier change for the industry to adopt Cobalt as a new metal.

So I'll move to Slide #11 and show you where Cobalt will be introduced. And this is the -- about a 10-nanometer cross-section, which is seen over here. And on the left-hand side, you'll see the layers marks. And so we've got the transistor contact. This is the -- this is typically done with tungsten and this makes contacts to the transistors. Above that, you have the various interconnect layers, typically done with copper and we've marked out over there the MgO, M1, the 2 smallest copper interconnects. As you can see, in the yellow text on the left-hand side. So at the 10-nanometer node, you have 1 layer of tungsten and the rest are made with copper. At the 7-nanometer node, we expect -- we will see these option of Cobalt required to get better performance out of these transistors, and we'll see Cobalt adopted at the transistor contact level and as well as for 1 or 2 of the local interconnect levels, as you can see there.

So I want to move to Slide #12 and give you some sense of what kind of impact we should expect to see from this Cobalt transition. So the graph over here shows the -- on the left -- on the x -- on the y-axis, a conducting metal width and on the x-axis, a critical dimension, as you see over here. Tungsten requires, as you can see over here, tungsten is shown in the lower figures, requires a pretty thick sleeve. This is shown in green. This is, in the industry, called the line on the barrier. It requires a quite a thick line on barrier in order to fabricate a tungsten contact. And these liners and barriers are typically shrunk as small as it can get. And so when you need to shrink the critical dimension, the only place to shrink is the actual tungsten metal inside the contact, and the line over there shows the conducting metal with in those tungsten contacts, going down from 8 to 3 at the 50-nanometer critical dimension and then essentially getting to 0 as a 12-nanometer critical dimension.

Cobalt, on the other hand, can work with a much thinner sleeve, a much thinner line on barrier. You can see, as denoted by the much thinner green line or on the blue Cobalt metal. And as a result, for the same critical dimension has a much larger conduction volume. In fact, at critical dimension of about 15-nanometer CD, which is approximately where the 7-nanometer transistor contacts are, there's a 3.7x increase in the conducting volume, and this should translate directly to a huge improvement in performance for that contact. And just to get my point across again, you can think about this as a tungsten transistor contact trying to drink -- trying to drink your morning smoothie with a coffee stirrer or straw with this Cobalt going back to a regular straw. So certainly a much more satisfying situation. And for the semiconductor industry, terribly important thing to try to extract performance from these transistors.

If you move to Slide #12, I'd like to explain why this is -- why Cobalt replaces copper. And it does so for different -- in the same but for different reasons. Now turns out even copper local interconnects are starting to throttle performance for a transistor. And when dimensions are large, as you could see at the left-hand side, the 2 graphs at left-hand side, when dimensions are larger, copper happens to have a lower resistance compared to Cobalt. However, as these dimensions shrink, there is a crossover, at which point Cobalt has a lower resistance to copper. Now this is kind of a little bit counterintuitive, but there's a good reason for this. And the reason for this has to do with how electrons move within metals. And we have an animation posted on the website, if you like to review later. But on copper, electrons have a wide mean free path, around 40 nanometer, which means that they move in a wider wave, bouncing inefficiently at the surface of these narrow lines. And this slows them down and creates higher assistance. In contrast, in Cobalt, the electrons mean free path is around 10 nanometers, and electrons essentially shuttle down the narrow line with fewer collisions at the -- with the surface, resulting in a lower resistance to the current flow. So this gives Cobalt a lower resistance than copper at smaller dimensions. But again, if you need a pictorial, think of a 100-meter sprint being -- copper represented by a man who's had more than a few drinks, finding a meandering path to the finish line. And Cobalt, represented by, say, maybe, Usain Bolt, making lightning-fast straight path to the finish line. Of course, Cobalt -- electrons going from Cobalt are going to get there faster. There's one more reason for the difference actually. As I mentioned earlier, Cobalt can work with thinner barriers than copper. And as a result, the vertical resistance was also lower. So you can see on these 2 pictorials, the sleeve or the liners that are used to contain the copper metal are much thicker than the ones that are usually contain a Cobalt metal. And as a result, the resistance through that contacting interface is much lower for Cobalt. All these mix, replacing copper with Cobalt is, sort of, a requirement to unlock the full potential of the transistors at these smaller dimensions.

So with that background, I want to move to Slide #14. And just give you some numbers just to, kind of, what kind improvement we'll see for Cobalt. In this case, for Cobalt replacing tungsten for the transistor contact. And the graph shows the transistor, the normalized transistor contact resistance on the left-hand side on the y-axis and compares tungsten and Cobalt. As you can see, the new formed Cobalt -- sorry, from tungsten, which has, in this case, a median normalized resistance of 8.59. The Cobalt resistance for the same contact, this happens to be 50-nanometer contact, whole is about 1. So huge reduction, I think 80-or-some percent reduction in the resistance. And this is -- this directly translates into the ability to extract power and performance out of these transistors. Also, if you noticed another very important point is the variability. With the tungsten contacts, there's a very large variability. Again, this variability, you can think of as affecting the speed of these devices and essentially going to be as fast as the slowest device and the improved variability again gives you better performance margin at these smaller dimensions.

So with that, I want to move to Slide #15 and tell you something about how Cobalt delivers performance improvements at the -- at a chip level. And we've done this a little simplistically, but we -- we've done this using some EDA simulation tools. So before I say that I just want to say, to better judge the value of Cobalt, we've actually been using tools, such as these EDA tools -- EDA simulation tools to figure out whether what kind of value we might get from these and get from these kind of changes. And these are big changes that we're making over here. So on the left-hand side, what you're looking at, is a 5-transistor ring oscillator circuit setup. This compares the performance loss for the tungsten transistor contact with that of a Cobalt transistor contact. And for simplicity, we've excluded the change in the metal M1 effects for -- and for this purpose we're just using copper. This is part of our Products Development Engine. This is the stuff Gary talks about in how we do developments within the company, and that's our own internal systematic approach to developing new products. It's an excellent way for us to judge the value for project, especially something as significant a change as this prior to making a major investment. So we see on the right-hand side that for every critical dimension that we've modeled here, Cobalt has a higher performance -- Cobalt contact has a higher performance than a -- than these ring oscillator circuit with the tungsten transistor contact. In fact, the benefits of Cobalt increase has these dimension shrink and get almost up to or get up to 15% improvement relative to a tungsten contact. So a very significant improvement in chip performance, as these dimensions shrink.

So I want to move to Slide #16 and provide some explanation on how we do this. So this Cobalt integration is enabled -- or this process enabled through a variety of processes across multiple platforms and technologies that are available within Applied Materials. To begin with, we're using the Endura platform to do a surface breadth -- and by the way, we have a animation. These are stills from the animation. There's an animation on the website you can look at. So I begin with the Endura platform to do a clean titanium deposition, an ALD metal barrier, PVD Cobalt as an anchor layer and then CVD Cobalt as a filling metal. Follow that up by an anneal that's down on the producer. This is the first time we are launching an anneal product on the producer. This anneal is done -- the purpose of this anneal is to purify the film to help the Cobalt metal move, flow into these small features and to also help the Cobalt greens grow large in order to get a lower resistance.

We follow that up with another PVD Cobalt layer that's used to deposit a thick oil burn to prepare the wafer for planarization and then goes into our Reflexion LK Prime tool to planarize to CMP, and we've also developed special tools in the PROvision to analyze these features and to study

the perfection of the fill and so on. So it utilizes 4 of our platforms and just a wide range of technologies to create this integrated metal solution. And I think at Applied, we are uniquely positioned to do this kind of work because it does take a very wide range of technologies in order to bring these new materials to the market.

So with that, I'm sure you have some questions on what impact this has for us. So this next slide, Slide #17, shows a place in my chart of the change in the opportunity going from the 28-nanometer node typical chip to a 7-nanometer node typical chip. As you can see on the left-hand side, on the 20-nanometer chip, there was a tungsten transistor contact layer. There's one of those. There's about 10 copper layers and there's 1 aluminum layer at the -- on the right top of the chip. As we move to 7-nanometer, we anticipate about the tungsten layer at the transistor contact to go away. We anticipate about 1 to 3 layers of Cobalt, about 11 to 13 layers of copper metallization followed by the 1 layer of aluminum on the -- as the terminal layer. And the entire fam would have increased about 2.7x.

To give you some sense of how this -- would this -- some scale, Cobalt, in this case on the placemat is modeled at about 1.5 layers of Cobalt and that's about -- that represents about $100 million of opportunity, while the copper represents about a $500 million worth of opportunity.

So with that, I want to summarize this presentation today. So we really think, at Applied Materials, materials are ensuring the way forward to meet the -- to address the challenges with performance reductions with slowing Moore's Law. And this is needed in order to meet some of the biggest challenges that -- and the opportunities created by this AI wave. At Applied Materials, we are uniquely positioned to deliver these Integrated Material Solutions required to bring these new materials and structures to the market. We have approvals of the platforms that can be easily adapted to provide the solutions, and we have the broadest portfolio of engineering technologies to enable these capabilities basically.

And with that, we are done with the presentation and I'll pass it back to Mike.

Michael Sullivan - *Applied Materials, Inc. - VP of IR*

Okay, great. And thanks, Kevin, very much. So what we do know is we'll get ready to do the Q&A session. And I think what I'd like to do is just quickly summarize from my perspective to you. This is really about the Product Development Engine. I think a number of you have heard us talk about that over the years. It's something that Gary brought into the company and that is now used broadly throughout the company. What we've been showing you today is the product of 5 years of work. And so what it's really all about, is you've got to use your technology expertise to anticipate inflections and especially if the industry continues to try to shrink, it's getting hard. The materials that you are used to seeing, when you shrink them any further, they break down, they don't work, they slow things down, they get worse. And so what we really need to do if we're going to continue to shrink is we've got to shrink and change the materials and that's our job. So what we are doing with the Product Development Engine is we are anticipating these inflections. It takes a long time to adjust the solutions. This took 5 years. But we're -- that's what we do every day. When we talk about a road map that we have that's building, this is a great example. When we talk about earlier in deeper collaborations with our customers, that's exactly what's going on right now, because the technology is getting so hard that there's 2 choices, either the road map slows down or we go faster. So we're going to go faster.

The idea of anticipating the inflection is that we want to be the first company that is there and ready to help our customers with a complete solution that can help them speed things to market. That's the goal, that's what you're seeing today. And we have 2 assets that really help us here: number one, we mentioned these platforms, we don't often talk about them, but we have things like Endura and producer. You will find these in every fab around the world. We've shipped around or over 5,000 of each of these. So every chip is made with these and these have become not a single process system anymore, these are multiprocess systems. And sometimes they're highly, highly integrated, not only inside the machine, but with other related steps. This is what it takes today to compete and to keep customers driving Moore's Law.

So that's what we're doing, and I think the other thing that's really important is breadth. There was a time in the industry we're doing one thing well, was exactly what customers needed. It was what gave you success. We argue that we're in a industry environment now where breadth is what customers need. Breadth is what we can use to help customers to continue to push the road map as Moore's Law classic shrinking gets harder and harder.

And so what you saw from Kevin on that one slide is the breadth that we have. You saw cleans technology. If you looked at the Gartner road map, you'd see that Applied is not in the cleans business according to Gartner. You saw ALD technology on the producer platform. If you looked at the Gartner data, you wouldn't see us in ALD technology. That's because we have these technologies. They typically have been characterized as PVD when they're shipped. But that's not what we have. So we have a much broader portfolio than people realize. We're integrating in a new wave, and we think that, that's going to be increasingly differentiable for Applied Materials, and we think that as we go forward in the industry from these more simple eras of engineering to the more complex eras of engineering, that this is exactly the way forward. So we're really excited about this. We're excited to be working on something for 5 years and to be able to share it with you. And what we'd like to do now is just kind of pause, get things back to the operator and see if anybody has any questions. If you have a question and you rather not share it, just send an e-mail and we'll get back to you later. But if anybody has a question that they'd like to address on the call, now is a great time. Thank you.

QUESTIONS AND ANSWERS

Operator

(Operator Instructions) Our first question comes from the line of Atif Malik with Citigroup.

Atif Malik - *Citigroup Inc, Research Division - VP and Semiconductor Capital Equipment & Specialty Semiconductor Analyst*

On Slide 17, you guys are showing how of your SAM grows moving from tungsten to cobalt. And my understanding is your position in tungsten is not as strong, so moving to cobalt definitely helps your opportunity. The question is, are there other ways than physical vapor deposition to put cobalt in the interconnects like electroplating? Or you think physical vapor deposition is the way to go to deposit cobalt? And then I have a follow-up.

Kevin Moraes

Atif, this is Kevin. So actually, you're right. There are multiple ways to deposit cobalt. Physical vapor deposition is one of the ways that we use. We also use CVD, chemical vapor deposition, to deposit cobalt. Another way that, that's been looked at in the industry is ECD as well. However, in these -- to enable these cobalt contacts and cobalt interconnects, we find that a combination of the PVD, the physical vapor deposition, and the chemical vapor deposition cobalt is essential. The physical vapor deposition cobalt is required in order to get good reliability because it help stacks an anchor layer at the bottom of these features. The chemical vapor deposition, CVD, is required in order to get a nice conformal cobalt that can then be flowed and filled into the feature. And so these are really the primary ways to get your cobalt fill. There was, as I mentioned, also a third step which we do a cobalt step at the very end as a over burden layer. Again, that can be done with PVD or that might be done with ECD as well. That's a less critical step in the entire process.

Atif Malik - *Citigroup Inc, Research Division - VP and Semiconductor Capital Equipment & Specialty Semiconductor Analyst*

Great. And as a follow-up, in terms of the adoption of cobalt, is it across all foundries, logic makers? And also, if you can talk about the memory makers, when they can move to cobalt? And the reason I ask this question is, one of the microprocessor companies is struggling with yields and -- because of the packaging and application, is this going to be kind of a driver to improve their yield performance or slow them down. If you can just talk about the kind of the diversity of cobalt adoption across foundries and logic makers?

Kevin Moraes

Sure. Atif, I can speak in general terms, I can't speak to specific customers or how they might be doing in terms of yield and what might be solutions to that. But, yes, so as you saw, cobalt is primarily being introduced as a performance enhancement. And where the performance most is in these logic and foundry type of devices. So that's where you're going to see the adoption initially. But as with any new metal, you start -- the adoption starts one place and then it slowly migrates into other places. I mean, memory didn't move to copper interconnects for many, many years after

logic adopted copper interconnect. It seems there's sort of an overkill, but today, all memory customers use copper interconnects. That said, at this stage, the cobalt adoption is starting with the logic foundry customers at sort of the 7-nanometer foundry node dimension size. That's where as you saw there's a huge performance incentive to move from tungsten to cobalt, yes. Was that -- does that answer your question, Atif?

Atif Malik - *Citigroup Inc, Research Division - VP and Semiconductor Capital Equipment & Specialty Semiconductor Analyst*

Yes. Very helpful.

Michael Sullivan - *Applied Materials, Inc. - VP of IR*

That's great. And Atif, you know, one other thing I'd mention is that, I think, that this approach that we have here, you're going to be hearing about this term more and more in the future, Integrated Materials Solutions. This is pretty new for us. And what you'll see is that this is not limited to what we're doing today with cobalt. It's going to be used in other areas as well. And a good example of that is going to be patterning, actually. And so we are -- as you know, as the company growing in SADP, SAQP patterning and we're anticipating the arrival of EUV technology, for example. And as we discussed at the ISS event in January, that lithography improvement does not by itself help to make the chips work. We're going to need to -- we're going to be moving increasingly to 3D structures. Even in logic that need to be aligned and the scanner doesn't take care of the overlay problem by itself as the customers have pointed out. And so what you need is materials-based self-alignment schemes, whereby we can create selective regions in the chip, such that if the scanning is off a little bit on the layer that needs to connect to the layer below, we can actually make it such that the materials will make sure that, that VR lands exactly where it needs to be. That's an extraordinarily complex materials engineering feat. It involves many, many selective steps. It includes many, many CMPs. And in a single layer, we'll have 5 CMPs and a whole bunch of selective steps. So that's brand new technology. And to do that, we need to bring together about 5 different equipment types at Applied. So that's the kind of thing that going forward will help drive the roadmap together with EUV and other techniques is going to be necessary. So stay tuned for more of that.

Operator

Our next question comes from the line of Harlan Sur with JP Morgan.

Harlan Sur - *JP Morgan Chase & Co, Research Division - Senior Analyst*

I believe that Intel is one of your major customers, is already using cobalt approach for their first 2 interconnect layers at their 10-nanometer process node. So great to see the adoption here. I know you touched upon foundry, but based on what we know at the 7-nanometer nodes, I don't think any of the foundry suppliers are actually using cobalt at the M0 and M1 interconnect layers. So is this more of a kind of a 5-nanometer adoption curve for the foundries?

Kevin Moraes

Yes. So actually, we can't speak to what customers, again what customers might be doing. However, as you have noted, there have been some public announcements by some of the logic foundry customers as to what they might be doing. And so I think we'll leave that out in the -- that's what's out in the public domain. The actual approach that each customer might take would depend. The cobalt, as I mentioned, is kind of a -- as a replacement to the conventional tungsten tranche to contact is sort of slam dunk. There's a massive amount of gain to be achieved there. And so it's likely that's, that's going to be the first place where you see adoption. And the benefit of it decreases as you go higher and higher up into the interconnect circuits. Then it's a matter of customer's design rules and ultimate technology that might be available to address loss or performance loss from resistance in these, say, M1 and -- M0 and M1 interconnects as an example. In addition to that, we happen to have other technologies that we haven't -- that we're not announcing basically, that are also improvements on the status quo, basically, of technologies that we use above. So it's possible cobalt may be 1 layer in some cases, may be 3 layers in other cases. So it's all over the place, depending on the customer's device and the process that they happen to be using at that particular fab.

Harlan Sur - *JP Morgan Chase & Co, Research Division - Senior Analyst*

Great. And you know you did a great job of highlighting the circuit performance benefits of moving to cobalt. Can you maybe just help us understand from a manufacturability perspective, right, metrics like process module throughput, defectivity, total cost per step of using cobalt process relative to, let's say, competing copper or tungsten process flows?

Kevin Moraes

Sure. So from a manufacturability standpoint, so as I mentioned, cobalt essentially provides a much larger window for gapfill. And this is for basically getting a reliable contact that can shuttle a lot of electrons to it. So compared to tungsten, just given the -- given how small these features have gotten and how limited the amount of tungsten metal is available in them. So if you have any variability in your transistor contract feature size, that's going to translate into huge variability in the tungsten metal and an even more dramatic variability in the resistance. So cobalt, by giving you that much higher margin essentially gives you that as an improvement in overall process margin. That's one aspect of the process margin. In terms of defectivity and so on and so forth, these are things that have been worked out to help with the adoption of cobalt. There are different kinds of defectivity for tungsten as for cobalt, but that's not a showstopper. In terms of the cost of -- or to give you a sense on the cost of the cobalt versus tungsten, cobalt is a more expensive process. It's about 4x more expensive than the tungsten flow. But there is a -- we're not focused on -- we're focused on delivering value to our customers and there is a huge performance benefit arising from these cobalt contacts.

Michael Sullivan - *Applied Materials, Inc. - VP of IR*

And I would want to add to that. So you're talking about which customers are interested in cobalt today versus others. I think a really key point that's worth underscoring is that the node names really no longer reflect the physical reality of what the customer's design rules are. And so what you're going to see is that some customers are going to experience copper and tungsten hitting the wall before others do. And -- but overtime eventually, I think what you're going to see is that cobalt will be adopted by most customers as they continue to try to shrink. And for that reason, we have the Maydan Center in Sunnyvale, California, that's the 300-millimeter development fab for customer collaboration. And today, we have people living there full time, working on these future nodes. So that's where we're trying to get these problems sorted out and the roadmaps configured for the future.

Operator

Our next question comes from the line of Timothy Arcuri with UBS.

Timothy Michael Arcuri - *UBS Investment Bank, Research Division - MD and Head of Semiconductors & Semiconductor Equipment*

I had two questions. First of all, from a competition perspective, the path to cobalt, I think has been pretty good for maybe 4 years or so. Obviously, Intel has led the charge and even GLOBALFOUNDRIES recently has made some public comments about using it. And I think you had Endura Volta for CVD Cobalt out for a while, probably 3 or 4 years now. So my question is, do the competitors like TEL and Lam, do they offer the same type of cobalt solutions? Can you give us a little bit of kind of a competitive update?

Kevin Moraes

Thanks, Tim, for that question. So, yes, we've been looking on cobalt, as you mentioned, for quite a long time, in fact, we released a cobalt process in about 2012, if I remember correctly, the Volta cobalt process and that was for the cobalt liner application for copper. In other sense, that was just an enhancement to the conventional copper interconnect. So we've been in the cobalt business for a very long time. And actually, we've started -- our development in cobalt started many, many, many years before that. So we've got the widest experience with cobalt. Depositing cobalt with CVD, understanding this material in terms of how it behaves, having a variety of processes, for example, the PVD processes, physical vapor deposition

processes or the annealing processes and also proprietary inspection processes we developed to study these. So we've got the best process knowledge on how to develop new processes, develop new integration schemes, study the effectiveness of these, and to deliver solution to our customers. So we're kind of well ahead of that for cobalt than any of our competitors. None of our competitors have a solution that comes anywhere close to what we have, and in terms of creating the value that we create with this cobalt solution compared to what we have. So no competitor today, for example, has a viable or a production-proven CVD Cobalt solution as an example. And that's also critical component, along with the PVD, physical vapor deposition, cobalt, the critical components of making this cobalt integration work.

Timothy Michael Arcuri - *UBS Investment Bank, Research Division - MD and Head of Semiconductors & Semiconductor Equipment*

Got it. Okay. And then just a follow-up on Slide #17. Can you help isolate cobalt in terms of what the actual expansion is of the SAM, just from cobalt. I know that there is, as you mentioned, some like e-beam solutions that are optimized for cobalt. But what is the expansion in the SAM that's specifically related to cobalt?

Kevin Moraes

So actually the -- what we showed here is really the expansion in the SAM. So the numbers that we've shown here, they relate only to the deposition tools and the annealing tools, which are brand-new process modules for the fab. The planarization tool is a new process on a proven system and the inspection is also some modifications to our PROVision system. So the numbers that we've shown here actually are the more conservative expansion numbers, not including the fact that the other layers are growing for planarization and for inspection. So to give you some more information on that, as I mentioned earlier, the cobalt versus tungsten, it's about a 4x increase in the TAM for us. And the cobalt versus copper is about a -- just cobalt versus conventional copper is about a 3x increase in TAM.

Michael Sullivan - *Applied Materials, Inc. - VP of IR*

Tim, just some rough numbers too. I mean, we thought about the 28-nanometer node and the 7-nanometer node, so what you see here is that the tungsten is going away. That's not our market, so that's okay. The cobalt is growing quite a bit. And if you think about the bar on the right of that, that area, that's well over $0.5 billion of market for us in just those spaces. So again, this is excluding the CMP, the inspection, the metal gate, et cetera. And the cobalt portion is well over $100 million already, even though this is a new technology. And as you know, because you've been watching this industry probably as long as anybody, once these things start, they have the tendency to proliferate. And so we think this will be a business that scales into the multiple hundreds of millions of dollars. And you probably also know that where these technologies are being combined, they're being combined on platforms that are very sticky in terms of their use by customers and the technologies that we're hanging on these platforms in order to do this are what we refer to as our leadership products. So these are these products where we have very, very strong product positions and pretty darn good business.

Kevin Moraes

Let me offer 1 more clarification that's actually on tungsten. Now the -- from a tungsten and copper standpoint, the business, as you know logic side is split. And in some cases, we are -- we're placing our own business with a more valuable business and in other cases we actually will place in the competitor altogether.

Michael Sullivan - *Applied Materials, Inc. - VP of IR*

Operator, do we -- if we have time for maybe one more question.

Operator

Our last question comes from the line of Edwin Mok with Needham & Company.

Yeuk-Fai Mok - *Needham & Company, LLC, Research Division - Senior Analyst*

First, I guess, I should try and understand where the cobalt market is right now versus where -- kind of where we think it will go. As you mentioned, cobalt has already been in the liner area for a while, right? How much adoption have we seen for that? And then as we make this transition from liner to actual doing it metal M1 -- M0 and M1, right? Are you kind of leveraging those positions that customer's already adopt that into kind of growing that? Or is it more just kind of greenfield for new customers? And I've a follow-up.

Kevin Moraes

All right, Edwin, thanks for the question. So cobalt actually is very well-integrated in the marketplace already for the copper interconnect application. As you've probably seen in customer announcements, that actually has been adopted by different customers at different times. The earliest adoptions probably are the 20-nanometer node and on the foundry side. And there have been more recent announcements by other customers. So cobalt as a liner for the copper interconnect is very secure and well adopted. Now again, cobalt as a liner for copper are sort of essential in order to extend the copper interconnect technology, both from a gapfill standpoint that's bottom for yield, as well as from a reliability standpoint because of electro migration issues with the conventional copper scheme. So cobalt is, on its own, as a liner and copper has been a very successful business for us. So -- and the other thing with that is that, that cobalt process is now -- that customers and well adopted and understood by customers and they're very comfortable with that. So we're actually building on that cobalt technology to this -- to make this cobalt interconnect scheme over here, the cobalt contact scheme here. It's actually just a building up on those with additional processes to enable transistor contact and interconnect cobalt filled schemes.

Yeuk-Fai Mok - *Needham & Company, LLC, Research Division - Senior Analyst*

Okay. Great. That's helpful color. And then just a follow-up question on the anneal process you guys highlighted on the Producer platform. Can you kind of give us a little color on that? Is that a RTP or even the second anneal held process? Or is it a slower -- like how slower annealing process?

Kevin Moraes

Yes. Edwin, actually, it's not an RTP. So because cobalt is being used in sort of a logic, middle of line, back-end theme, the thermal adjustor are much slower. What it really is, it's a sort of a medium temperature process. What's critical is ambience. What's critical is the thermal treatment time-temperature history. And that's what it's designed to do. So it's designed to really do a great job with excellent footprint density throughput and performance in terms of annealing, probably finding these cobalt films, growing this cobalt layer, cobalt crystals and so on and so forth. Hopefully, that answers your question.

Michael Sullivan - *Applied Materials, Inc. - VP of IR*

And so I think what we'll do is we'll end the call. Before we do, I've being getting a couple of e-mails over the past couple of days about SEMICON West. So I thought I might just take a moment to summarize what we're doing. So what you've seen in past years is we've used the Monday, July 9, we're actually going to, based on the investor feedback, to Tuesday, July 10. And we will be in San Francisco and not Santa Clara this year. And here's what we're going to do. So I think we all know the new AI era is happening all around us and what that means is we're having this data explosion, right? Data is growing 25% compound, but it's happening as Moore's Law is slowing. That's become evident over the past year, over the past few months, that's a new phenomenon in the industry. And so that creates a problem. It also creates an opportunity. And so what we're going to need in the industry going forward, is we're going to need new computing architectures that can do not single thread performance increases but orders of magnitude increases in data throughput for machine learning and data processing. And we're also going to need new

devices and especially new materials because the materials we've been using, they're not working anymore as we shrink. So what we're going to do at SEMICON West is, we're going to have an investor breakfast at 8 o'clock, but then we are hosting with SEMI a new event called the AI Design Forum and the idea is to create the first event ever where we -- to look at the whole ecosystem, from the materials on the wafer all the way to the new systems and explain all of the pieces and how they're going to fit together and how the industry is going to collaborate to make this work because it's going to take a lot of teamwork. What you're going to see is a lot of experts in -- from academia and from industry. So you'll be seeing people from Stanford; from Berkeley; IBM, John Kelley, who's their Head of Research; Qualcomm, a gentleman who's there who formerly was at Microsoft doing this kind of work, another Microsoft speaker, Applied will be there. So all of these companies will be there. We'll also have a lot of experts. David Kanter, you may know, who used to be at microprocessor report. Yan Borodovsky, you may know as one of the world's experts on lithography and what it takes to make EUV practical. Paolo Giorgini is going to be there. When he was at Intel, he was in charge of the 450-millimeter roadmap, which as you know has not materialized, but he's got a lot of ideas for where we're going from here. There will be other companies as well that are commercial companies. We also have start-up companies. So Sensient is a company that's a startup, it's going to do a bunch of edge devices. Cerberus is going to be there, they're going to talk about what they're doing in AI and how they're using silicone in some new ways. And then what I'm also very pleased about is that we're going to have a special event at around the lunch hour. We are going to celebrate the Turing Award that's been won by John Hennessy, who's from Stanford and now Chairman of Alphabet, along with Dave Patterson, who is from Berkeley and now at Google Brain. And the 2 of them wrote the textbook that everybody has used over the decades in commuting and they've won the Turing Award for their work on RISC, the microprocessor design. So Dave Patterson will be there. John is traveling, but Dave will be there. He's going to do a fireside chat, the latest edition of their textbook has a new supplement on AI and accelerated computing. So we'll talk about that. He will be interviewed by John Markoff, who you may know, he is the author who just wrote the big book on AI and he's been a writer for The New York Times for 28 years. And then that will lead us with the Bulls and Bear panel. That will be a little different this year. SEMI tells me that it'll be a lot more -- a little more systems-oriented, not just semicap, and that will be moderated this year by Don Clark. Many of you know Don, he was the Wall Street Journal reporter for many years and he now writes for The New York Times. So that gives you a sense of the day. We've realized that that's a big footprint on Tuesday. That's a big day. And so what we will certainly do, first of all, hopefully, this is appealing to many of you. Number two, we will hang around. So we'll stay around for Wednesday at SEMICON West. If you would like to meet us, meet us with us some of your clients. We'll make Wednesday a big day as well. And hopefully, we don't absorb too much of your footprint and we make it a great event. So thank you for your interest today and today's topics. Thanks, Kevin Moraes, and your team. We're really proud of what you've accomplished and we know that the pipeline is deep and this is just the beginning of change for us here. And we'd like to thank all of you for your continued interest in Applied Materials.

Operator

Ladies and gentlemen, thank you for your participation in today's conference. This concludes the program, and you may now disconnect. Everyone, have a great day.