



Xilinx 7 Series Domain – Platform Launch

Demo Descriptions

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Xilinx and its Alliance Program Members have put together a series of video demonstrations to help customers understand the benefits and capabilities of the first Kintex™-7 FPGA and Virtex®-7 FPGA development kits. Below are the links and descriptions of each demonstration. All Xilinx videos can be found at: <http://www.youtube.com/XilinxInc>.

[Kintex-7 FPGA DSP Kit with High-Speed Analog Demonstration](#)

Jointly developed with Avnet Electronics Marketing, the Kintex-7 FPGA DSP kit with high speed analog is a DSP Domain Targeted Design Platform for the development of high-performance signal processing applications. This short video provides an overview of the KC705 baseboard and FMC150 analog interface hardware and a description of the Kintex-7 325T FPGA. A Targeted Reference Design is downloaded and executed in the hardware to perform digital up/down conversion to the analog interface connected in a loopback configuration. We then progress to a second design that demonstrates a new level of platform integration to the MathWorks model based design environment. The integration allows real-time analog data from the data converters to be buffered and brought into the Simulink® environment for analysis and design development using the Xilinx System Generator tool or HDL Coder.

[AMS Evaluation Card Demonstration](#)

The Agile Mixed Signal evaluation card supports two methods for supplying the analog signal source. Connected to the Kintex-7 FPGA KC705 base board in this demonstration, the AMS card supplies the signal via four independent BNC connectors, which interface to traditional analog function generators or other analog hardware. The second method is via an on-board digital to analog converter (DAC), which outputs an analog signal. Either of those signals can be multiplexed and buffered across the 20-pin connector cable, which is then routed to the XADC inputs on the FPGA.

[Xilinx Power Advantage featuring KC705 Evaluation Kit Demonstration](#)

Xilinx set out to make unprecedented reductions in power at the 28nm process technology node by reducing static, dynamic and I/O power while optimizing everything from the process itself to the ISE® Design Suite tools. Xilinx worked with foundry partner TSMC to develop the HPL (high-performance/low power) process used on all its 7 series FPGA and Zynq™ EPP families. The HPL process offers Xilinx 50 percent lower static power than competing FPGAs without sacrifices in performance. In addition to process innovations, Xilinx also added dynamic shutdown capabilities in the I/O to reduce wasted DC power for memory interfaces. This

demonstration shows how dynamic power is reduced with use of the intelligent clock and logic gating features in the ISE tool. This simple switch in the tool takes advantage of local and global enables to gate off unnecessary toggling and save dynamic power, thereby reducing total power.

[Kintex-7 FPGA DDR3 Interface demo](#)

This demo demonstrates the Kintex-7 FPGA interface capabilities to DDR3 memory. It shows how easy it is to get the high performance 1600 Mbps DDR3 design ported to a hardware platform and this example is available today. These capabilities provide the user with a jump start to their DDR3 portion of the FPGA design to accelerate their overall time to market. The reference design featured here is a standard IP that is freely available through the Memory Interface Generator (MIG) IP core. The reference design has been ported to the Kintex-7 KC705 platform. The demo is also using the ChipScope™ Analyzer software to demonstrate the functionality of the interface and DDR3 controller. It provides the capability to test and verify the functionality of the DDR3 interface that is running at 1600 Mbps between the FPGA and the DDR3 64 bit SODIMM on the KC705 board included with the Kintex-7 FPGA development kits.

[Kintex-7 FPGA KC705 Evaluation Kit with AMS HMI Touch Screen Demonstration](#)

As part of the 7 series Targeted Design Platform Launch, Xilinx is highlighting the Agile Mixed Signal (AMS) technology featured in all its 28nm devices to provide designers with a flexible, general purpose analog interface. This video uses an HMI Touch Screen application to demonstrate the capabilities of AMS. The simple, 4-wire touch screen application demonstrates the capability to move signal conditioning from the analog domain into the digital domain and leverage the flexibility of the FPGA.